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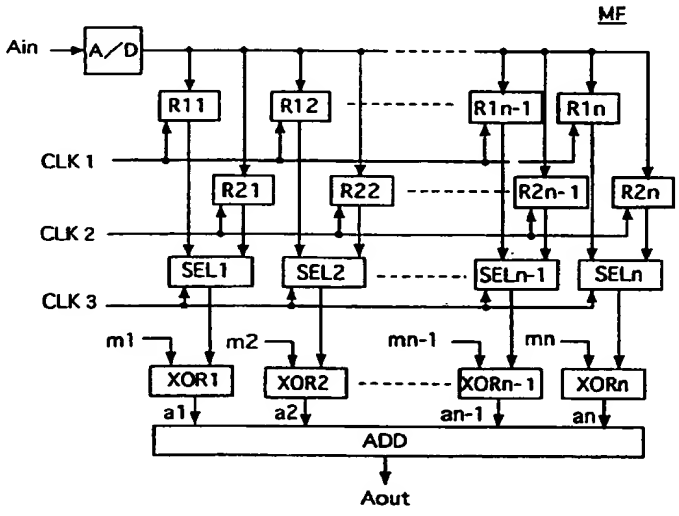
(54) Matched filter and signal reception apparatus

(57) An analog input signal is converted into digital data by an A/D converted, a digital multiplication as a correlation calculation is executed by a plurality of exclusive-OR circuits, and an analog addition of outputs of the exclusive-OR circuits is performed. In the multiplication, the digital data is multiplied a spreading code of one bit. The exclusive-OR outputs are added for each weight of bits, and the addition results are weighted and summed up.

Fig.2



EP 0 939 500 A2

Description

Detailed Description of the Invention

Background of the Invention

Field of the Invention

[0001] The present invention relates to a matched filter and signal reception apparatus, particularly to a matched filter and a signal reception apparatus preferable for a DS-CDMA cellular system.

Prior Art

[0002] Recently, the direct sequence code division multiple access (DS-CDMA) cellular system attracts attention as the users of the land mobile communication increase, because the DS-CDMA system has large capacity. In the DS-CDMA system, at a transmitter side, the transmission data is modulated and then spreaded by a PN-code, and at a receiver side, the received signal is despread by the PN-code so that the transmission data is reproduced. A sliding correlator or a matched filter is used for the despreading. The sliding correlator is small in circuit size but needs a long time for the correlation calculation. While, the matched filter is fast in correlation calculation but is rather big in circuit size.

[0003] The conventional matched filter consists of a charge coupled device (CCD), a surface acoustic wave (SAW) device, or a digital circuit. A matched filter is proposed in Patent Publication Hei06-164320 by the inventors of the present invention, which consists of an analog circuit and is of high speed as well as low power consumption. The matched filter includes a sampling and holding circuit for holding a plurality of input analog signals as discrete data, a plurality of multiplication circuits for multiplying the analog signals by multipliers that are shifted and circulated and an adder for summing the multiplied data up.

[0004] However, the proposed matched filter has a problem of rather large circuit size because a lot of analog sampling and holding circuits and peripheral circuits such as refreshing circuit.

Summary of the Invention

[0005] The present invention has an object to provide a matched filter and a signal reception apparatus not only of low power consumption but also of small circuit size.

[0006] According to the present invention, a matched filter comprises an A/D converter for converting an analog signals into digital data, a data holding means having a plurality of stages for holding said digital data, a multiplier supplying means for supplying a spreading code, a plurality of exclusive-OR circuits corresponding to the stages, each of which calculates an exclusive-OR of one of the digital data and one of said 1 bit data, and an analog adder for summing said exclusive-ORs up.

[0007] In a matched filter according to the present invention, analog input data are converted into digital data by an analog to digital (A/D) converter and exclusive-or of the digital data and PN-code is calculated.

[0008] In another matched filter according to the present invention, analog input data are converted into digital data by an A/D converter and exclusive-or of the digital data and PN-code is calculated, then the exclusive-or output is summed up by an analog adder.

Brief Description of Drawings

[0009]

Fig.1 is a block diagram showing an embodiment of a signal reception apparatus for DS-CDMA cellular system using a matched filter according to the present invention;
Fig.2 is a block diagram showing a first embodiment of a matched filter according to the present invention;
Fig.3 is a block diagram showing a plurality of registers of PN codes in Fig.2;
Fig.4 is a block diagram showing a phase multiplexer in Fig.3;
Fig.5 is a diagram showing signal wave having an overlap of correlation peaks;
Fig.6 is a block diagram showing an analog adder in the matched filter in Fig.2;
Fig.7 is a block diagram showing an D/A converter of the analog adder in Fig.6;
Fig.8 is a block diagram showing another analog adder;
Fig.9 is a block diagram showing an inverting amplifier in Fig.8;
Fig.10 is a block diagram showing an exclusive-OR circuit;

Fig.11 is a block diagram showing another exclusive-OR circuit;
Fig.12 is a truth table of selectors in Fig.11;
Fig.13 is a block diagram showing a second embodiment of a matched filter according to the present invention;
Fig.14 is a block diagram showing a third embodiment of a matched filter according to the present invention;
Fig.15 is a block diagram showing an analog adder in Fig.14;
Fig.16 is a block diagram showing a sub-adder in Fig.15;
Fig.17 is a circuit diagram showing another analog adder for the third embodiment;
Fig.18 is a circuit diagram showing an analog adder used together with the adder in Fig.17;
Fig.19 is a circuit diagram showing another analog adder used together with the adder in Fig.17;
Fig.20 is a circuit diagram showing a MOS differential amplifier in the analog adder in Fig.19; and
Fig.21 is a block diagram showing another embodiment of a signal reception apparatus for DS-CDMA cellular system.

Preferred Embodiments

[0010] Hereinafter, preferred embodiments of the signal reception apparatus for DS-CDMA cellular system and matched filter therefor are described with reference to the attached drawings.

[0011] Fig.1 is a block diagram showing a main portion of a signal reception apparatus for DS-CDMA cellular system.

[0012] In Fig.1, 1 is a quadrature detector for separating an intermediate frequency (IF) signal into I- and Q-components by quadrature detection. 31 and 32 are matched filters according to the present invention, which despread the I- and Q-components, respectively, passed through low-pass filters 21 and 22, respectively. Despread outputs from the matched filters 31 and 32 are input to sampling and holding circuits 81 and 82, and to a level detection circuit 4.

[0013] The level detection circuit 4 calculates a signal power of outputs from the matched filters 31 and 32, and converts the signal power into a digital data output. The output of the level detection circuit 4 is integrated for a plurality of symbol periods by a recurrent integration circuit 5 in order to reduce influences of noise etc. The output of the recurrent integration circuit 5 is input to a peak detection circuit 6 for detecting peaks higher than a predetermined threshold. The output of the peak detection circuit 6 is input to a controller 7 for determining a timing of sampling and holding of the sampling and holding circuits 81 and 82, synchronous to the position (phase) of the peaks detected by the peak detection circuit 6. Thus, the I- and Q-components of the despread output corresponding peaks higher than the threshold are input to the sampling and holding circuits 81 and 82, respectively. The sampling and holding circuits 81 and 82 sample and hold the despread outputs from the matched filters 31 and 32 corresponding to the selected correlation peaks above. Outputs from the sampling and holding circuits 81 and 82 are detected by a coherent detection circuit 9, and are input to a rake combiner 10 which shifts the outputs in phase for synchronization and then combines the outputs. Output from the rake combiner 10 are input to an output interface (I/F) for generating a demodulated data (Data).

[0014] Fig.2 is a block diagram showing an embodiment of the matched filters 31 and 32. The matched filter MF includes an analog to digital converter (A/D) which receives a analog input signal Ain, one of I- and Q-components, output of which is input to a series of data registers R11 to R1n, and to a series of data registers R21 to R2n. The series of data registers R11 to R1n are controlled by a clock CLK1 so that one of the registers R11 to R1n receives the output of the A/D converter, successively and circulatedly. The series of data registers R21 to R2n are controlled by a clock CLK2, of the same frequency as CLK1 but shifted from CLK1 by a half period, so that one of the registers R21 to R2n receives the output of the A/D converter, successively and circulatedly.

[0015] A series of selectors SEL1 to SELn and a series of exclusive-or circuits XOR1 to XORn are provided corresponding to the data registers R11 to R1n and R21 to R2n. The outputs of the data registers R11 and R21 are input to the corresponding selector SEL1, the outputs of the data registers R12 and R22 are input to the corresponding selector SEL2, and similarly, the outputs of the data registers R1n and R2n are input to the corresponding selector SELn. The selectors SEL1 to SELn are controlled by a clock CLK3 so that each of the selectors SEL1 to SELn alternatively outputs one of the outputs from the series R11 to R1n and from the series R21 to R2n. The clock CLK3 is synchronous to the clock CLK1 or CLK2. When CLK3 is high, the data of the series R11 to R1n are selected, and when low, the data of the series R21 to R2n are selected. Each of the outputs of the selectors SEL1 to SELn includes a plurality of bits (LSB to MSB) and is input to the corresponding exclusive-OR circuit of XOR1 to XORn.

[0016] A series of spreading codes m1 to mn are input to inputs of the exclusive-OR circuits XOR1 to XORn respectively, and another input of each of the exclusive-OR circuits of XOR1 to XORn is corresponding to each output of the outputs of SEL1 to SELn. Each of the exclusive-OR circuits performs logical calculation of exclusive-OR of the corresponding output of the corresponding selector among SEL1 to SELn and corresponding bits of the spreading code. When the bit of the spreading code is "1", the digital bits corresponding to the analog input are inverted, and when " 0", not inverted. This is equivalent to a multiplication by the spreading code. The spreading codes m1 to mn are shifted and circulated in response to the clock CLK1, and are input to the exclusive-OR circuits XOR1 to XORn.

[0017] Outputs a1 to an of the exclusive-OR circuits XOR1 to XORn are input to an analog adder ADD for outputting

a total summation Aout of the outputs a1 to an. The outputs of the exclusive-OR circuits XOR1 to XORn are digital data, and the adder ADD converts the digital data into analog data so as to generate an analog data Aout as an addition result.

[0018] Since the circuit above performs the digital multiplication, the circuit size and electrical power consumption are reduced comparing with the conventional full analog circuit. The calculation speed of the present embodiment is fast and accuracy is high, because the multiplication outputs are summed up by the analog adder ADD.

[0019] The clocks CLK1 and CLK2 shifted by a half period from each other enable a "double sampling". When the double sampling is unnecessary, only one of the series of the data registers R11 to R1n and R21 to R2n is provided and the selectors SEL1 to SELn are omitted. Furthermore, more than two series of data registers may be provided for higher sampling rate.

[0020] Fig.3 is a block diagram showing a plurality of registers for supplying the PN code m1 to mn (multipliers) to the exclusive-OR circuits XOR1 to XORn in Fig.2. There are two systems for supplying the PN code, a first system from a calculation register CAL-REG1 and a second system from a calculation register CAL-REG2. Input registers IMP-REG1 and INP-REG2 are connected to the calculation registers CAL-REG1 and CAL-REG2, respectively. Different spreading codes Pa and Pb are input to input registers INP-REG1 and INP-REG2, respectively, and are transferred to the calculation registers CAL-REG1 and CAL-REG2, respectively. The last stages of the calculation registers CAL-REG1 and CAL-REG2 are connected to their first stages, respectively, so that the PN codes are circulated in response to a clock CK. The clock CK is synchronous to the timing that the data registers receive the outputs from the A/D converter. The CLK1 is used as CK, usually.

[0021] The data in the calculation registers CAL-REG1 and CAL-REG2 are input to phase multiplexers PMUX1 and PMUX2, respectively. The phase multiplexers output data in the CAL-REG1 and CAL-REG2, respectively, as they are, or of backwardly shifted state by one chip time. The outputs of the phase multiplexers PMUX1 and PMUX2 are input to a register multiplexer RMUX for alternatively outputting the outputs of CAL-REG1 and CAL-REG2 as MUXCNT. MUXCNT is input to XOR1 to XORn as the multipliers m1 to mn. By switching the register multiplexer RMUX, the correlation calculations by PN code in CAL-REG1 and CAL-REG2 are performed in time sharing manner.

[0022] As mentioned above, reception of long delay path more than one symbol period, of multi-code, and signal reception for soft hand-over are realized by a small circuit.

[0023] When the same spreading codes are input to the INP-REG1 and INP-REG2 of different phases from each other by a predetermined phase, a path delayed by more than one symbol period can be despread. When different spreading codes are input to the INP-REG1 and INP-REG2, signal reception for multi-code and for soft hand-over is possible.

[0024] There is a possibility that a plurality of correlation peaks by the PN codes stored in CAL-REG1 and CAL-REG2 occur simultaneously.

[0025] As shown in Fig.5, three correlation peaks P1, P2 and P4 occur by the first code in CAL-REG1 in a symbol period Ts. Two correlation peaks P3 and P5 occur by the second code in CAL-REG1 in a symbol period Ts. The peaks P4 and P5 occur simultaneously and will cause an overlapping of peaks. Since the phase multiplexers PMUX1 and PMUX2 output data in the CAL-REG1 and CAL-REG2, respectively, as they are, or of backwardly shifted state by one chip time as mentioned above, the overlapped peaks can be separated.

[0026] Fig.4 is a block diagram showing a phase multiplexer PMUX1 in Fig.3. The phase multiplexer includes a plurality of two-inputs-one-output data multiplexers DMUX1 to DMUXn corresponding to data D1 and D2, D2 and D3, ..., Dn-1 and Dn, and Dn and D1, respectively. By switching these data multiplexers synchronously, the data in the CAL-REG1 is output through the phase multiplexer PMUX1 as they are (current state) or backwardly shifted (one chip previous).

[0027] If no overlapping occurs as the peaks P1, P2 and P3 in Fig.3, the D1 to Dn in the CAL-REG1 are output as they are output. If the overlapping occur as the peaks P4 and P5, the correlation calculation by the spreading code in CAL-REG1 is once performed, and, one chip time after, correlation by the spreading code in CAL-REG2 is performed.

[0028] The control signal in Fig.5 is input to RMUX for alternatively selecting PMUX1 or PMUX2 in response to "1" and "0" of the control signal. In synchronism with the multi-paths P1 and P2, the control signal becomes high level "1" so that the RMUX outputs the first code stored in the CAL-REG1. Then, the data multiplexers DMUX1 to DMUXn output the data D1 to Dn as they are. Then, despread by the first code is performed.

[0029] The control signal becomes low level "0" for synchronizing with the peaks P3 and P5 so that the register multiplexer RMUX is connected to the phase multiplexer PMUX2. The signal is despread by the second spreading code stored in the calculation register CAL-REG2. Since the peak P4 and P5 overlap each other, one chip time after the despread of the peak P5 by the second code, the control signal becomes high level so despreading by the first code. The same received signal must be processed by these despread, the data multiplexers DMUX1 to DMUXn are switched so that the data backwardly shifted is generated.

[0030] The phase multiplexer PMUX2 is similar to PMUX1, so the description therefor is omitted.

[0031] If the data multiplexers are substituted by multiplexers of three-or-more-inputs-one-outputs multiplexes, data

before a plurality of chip times can be reproduced. A plurality of peaks overlapping, or a plurality of continuous overlapping can be separated. Next the adder ADD is described. Fig.6 is a block diagram showing an analog adder in the matched filter in Fig.2. The outputs a1 to an of the exclusive-OR circuits XOR1 to XORn are respectively input to corresponding D/A converters (M)1DAC for converting the digital signals a1 to an into analog voltage signals. Here, the data a1 to an are "M" bits signals.

[0032] Fig.7 is a block diagram showing the D/A converter of the analog adder in Fig.6, which includes a plurality of 1bit D/A converters 1bitDAC of a number of "M". The analog signals corresponding to the digital signals of XOR1 to XORn are input to the corresponding analog adders Adder1 to AdderM. Each of the dgital bits of outputs of the Adder1 to AdderM are added to other digital bits of the same bits, weighted by the weights and summed up by a weighted addition circuit.

[0033] Fig.8 is a block diagram showing another analog adder ADD. This analog adder directly adds the outputs of the exclusive-OR circuits XOR1 to XORn without the D/A converter. The adder ADD includes analog adders from 7_1 to 7_M for receiving the bits from MSB to LSB, and summed up with weighting by a weighted addition circuit 9. An output of the adder 9 is the total summation of the outputs of XOR1 to XORn.

[0034] The adder 7_1 includes a capacitive coupling consisting of parallel capacitances C11 to CN1 outputs of which are commonly connected to an input of an inverting amplifier 81. An output of the inverting amplifier 81 is connected through a feedback capacitance Cf1 to its input for compensating a linearity of the output of the amplifier with respect to its input. Here, inputs to the capacitances C11 to CN1 are X'11 to X'N1, C11=C12=...=CN1=Cf1/N , and an offset voltage of the amplifier is Vb, the output of the adder 7_1 is defined as in the formula (1).

$$Vo71-Vb=-\frac{\sum_{i=1}^{N}(X'i1-Vb)\cdot Ci1}{Cf1}=-\frac{\sum_{i=1}^{N}X'i1}{N}+Vb \tag{1}$$

The adder 7_2 to 7_M are similar to 7_1, so the descriptions therefor are omitted.

[0035] The weighted addition circuit 9 includes a capacitive coupling consisting of parallel capacitances C1 to CM, corresponding to the adders 7_1 to 7_M, outputs of which are commonly connected to an input of an inverting amplifier 10. An output of the inverting amplifier 10 is connected through a feedback capacitance Cf to its input for compensating a linearity of the output of the amplifier with respect to its input. Here, the capacitances C1 to CM have capacities proportional to the weights of MSB to LSB of the A/D converter, that is, 2^{m-1}, 2^{m-2},...., 2^2, 2^1,2^0. A relationship between Cf and C1 to CM is as in the formula (2). The output voltage Vo9 of the inverting amplifier 10 is defined as in the formula (3). Here, the input voltages to C1 to CM are V1 to VM.

$$Cf=\sum_{i=1}^{N}Ci \tag{2}$$

$$Vo9-Vb=-\frac{\sum_{i=1}^{N}(Vi-Vb)\cdot Ci}{Cf}=-\sum_{i=1}^{M}2^{i-1}\cdot Vi+Vb \tag{3}$$

[0036] Fig.9 is a block diagram showing the inverting amplifier 81 together with capacitances Cf and C11 to CN1. The inverting amplifier 81 includes three stages CMOS inverters INV1, INV2 and INV3 serially connected. A multiplexer MUX 6 is connected between the output of the amplifier and the feedback capacitance Cf, for connecting the Cf1 output to alternatively to the amplifier output or a reference voltage Vref. The input of the amplifier is connectable through a switch SW62, and Cf1 can short-circuited by a switch SW61. By connecting MUX to Vref and by closing SW61, the electric load of Cf is canceled for refreshing.

[0037] By connecting a gate input of INV1 to a ground and by opening SW62, the COMS inverters become sleep mode for preventing electrical power consumption. Multiplexers MUX11 to MUXN1 are connected to inputs of the capacitances C11 to CN1, for alternatively connecting C11 to CN1 to X'11 to X'N1 or to Vref. When refreshed, C11 to CN1 are connected to Vref.

[0038] A MOS resistance MR1 is connected to the first and the second stages of the CMOS inverters in the inverting amplifier 81, for reducing the total gain of the amplifier. A serial circuit of a MOS resistance MR2 and a capacitance CP6 is connected between the input and output of the last stage CMOS inverter for phase compensation. Unstable oscillation and unexpectedly large amplitude of the output is prevented.

[0039] As mentioned above, since it is possible to make the inverting amplifier 81 sleep mode by the switch SW62, the electrical power consumption is reduce at other timing than the correlation peaks by openig the switch SW62.

[0040] The calculation registers CAL-REG1 and CAL-REG2 are continuously shifting and circulating the data even when the inverting amplifier 81 is in a sleep mode for preventing the power consumption of the adder ADD. If the shifting and circulating are adjusted only for the correlation peaks, the continuous circulation is unnecessary. Then, the power consumption is decreased. In this case, zigzag type shift register is necessary for shifting the data to any stages in one clock. .

[0041] In Fig.8, the outputs of XOR1 to XORn are directly input to the analog adder, however, it is better to use high level supply voltage VH or low level supply voltage VL supplied from the outside, as shown in Fig. 10.

[0042] As shown in Fig.10, selectors SEL11 to SEL1M are connected to output of the exclusive-OR circuits X'1 to X'M, output of which are connected to capacitances at the input side of the analog adders. The voltages VH and VL, and reference voltage Vref are supplied to the selectors SEL11 to SEL1M which are controlled by the output-bit of XOR and a refresh control signal CR. When the output-bit is high level, the high level voltage VH is output, and when the output-bit is low level, the low level voltage VL is output. When CR is high level, the reference voltage Vref is output. In this circuit, voltages without noise are supplied to the analog adder, and the calculation accuracy is improved.

[0043] Fig.11 is a block diagram showing further another exclusive-OR circuit for diminishing the circuit size. In this embodiment, each selector outputs 4 levels voltage output in response to outputs of two exclusive-OR circuits XOR1 and XOR2. The number of inputs to the analog adder is a half of that of the embodiment in Fig. 10. The corresponding bits of the outputs X1 and X2 of the exclusive-OR circuits XOR1 and XOR2, and the refresh signal CR are input to the selectors SEL21 to SEL2M as the control signals. The selectors SEL21 to SEL2M output the voltages VH and VL according to the truth table in Fig.12. When the refresh control CR is high level, the reference voltage Vref is output regardless of the outputs from XOR1 and XOR2.

[0044] Since each of the selectors SEL21 to SEL2M outputs one voltage in response to two outputs from XOR1 and XOR2, the number of inputs to the analog adder is decreased to a half.

[0045] Fig.13 is a block diagram showing a second embodiment of a matched filter according to the present invention. Instead of the circulating input of the input signals to the data register in Fig.2, the input signals are successively input to shift registers SFREG1 and SFREG2 which shift the signals toward the trailing ends. The spreading codes can be fixed with respect to the stages of the shift registers. Outputs of the shift registers are input to selectors SEL1 to SELn to which exclusive-OR circuits XOR1 to XORn, and an adder ADD follow, similarly to the embodiments above.

[0046] Fig.14 is a block diagram showing a third embodiment of a matched filter in which the outputs from the A/D converter is a signed digital data. A digital data "a" indicative of an absolute value and a sign bit "b" are output from the A/D converter. The data "a" and "b" are parallelly input to series of registers R11 to R1n , or R21 to R2n, and one of the series is selected by the selectors SEL1 to SELn. The sign bits s1 to sn are input to the exclusive-OR circuits XOR 1to XORn, and a1 to an are input directly to the adder ADD2.

[0047] Fig.15 is a block diagram showing a analog adder ADD2 in Fig.14. The analog adder ADD2 includes a plurality of sub-adders ADD2S1 to ADD2Smcorresponding to absolute bits of the A/D converter. The outputs of the sub-adders are input to an summation circuit which includes a capacitive coupling having a plurality of capacitances C911 to C91M, a inverting amplifier INV91 connected at its input to outputs of the capacitive coupling, and a feedback capacitance Cf9 connected between an input and output of the inverting amplifier INV91. The summation circuit weights the outputs of the sub-adders with weights corresponding to the bit weights and sums them up. The capacitances C911 to C)1m have capacities proportional to 2^{m-1}, 2^{m-2},...., 2^2, 2^1,2^0, a relationship between Cf9 and C911 to C91M is as in the formula (4). An output Aout of ADD2 is expressed by the formula (5).

$$Cf9=\sum_{i=1}^{M} C91i \tag{4}$$

$$Aout\text{-}Vb=-\frac{\sum_{i=1}^{M} C91i\cdot(Ai\text{-}Vb)}{Cf9}=-\sum_{i=1}^{M} 2^{i-1}\cdot Ai+Vb \tag{5}$$

[0048] Fig.16 is a block diagram showing a sub-adder ADD2S in Fig.14. The sub-adder ADD2S1 includes selectors SEL91 to SEL9n to which exclusive-ORs of the sign bits and the multipliers are input as control signals. The reference voltage Vref and the absolute value data a1 to an are input to the selectors SEL91 to SEL 9n. The selectors SEL91 to SEL 9n introduce a1 to an to one of capacitive couplings, having capacitances C1011 to C101n or C1021 to C102n. An output of the capacitive coupling (C1011 to C101n) is connected to an input of an inverting amplifier INV101, output of

which is connected to its input through a feedback capacitance Cf101. An output of the inverting amplifier INV101 is connected through a capacitance CC1 to an input of the inverting amplifier INV102, and an output of the capacitive coupling (C1021 to C102n) is directly connected to the input of the inverting amplifier INV102. An output of INV102 is connected to its input through a feedback capacitance Cf102. ADD2S2 to ADD2SM are similar to ADD2S1, so descriptions therefor are omitted.

[0049] When the exclusive-OR calculation is "0" (positive), the selectors introduce the inputs to the capacitive coupling (C1011 to C101n), and when "1" (negative), to the capacitive coupling (C1021 to C102n). The sub-adders simply add the output bits, and execute the addition and subtraction shown by A1 in the formula (6). Here, C1011=C1012=...=C101n=C1021=C1022=...=C102n=CC1/n=Cf101/n=Cf102/n , and the formulae (7) and (8) are given.

$$A1\text{-}Vb=\frac{CC1}{Cf101\cdot Cf102}\sum_{i=1}^{n}\{(\overline{Si}\cdot ai+si\cdot Vref)-Vb\}\cdot C101i\ \frac{1}{Cf102}\sum_{i=1}^{n}\{(si\cdot ai+\overline{si}\cdot Vref)-Vb\}\cdot C102i \quad (6)$$

$$=\frac{1}{n}\sum_{i=1}^{n}\{(\overline{si}-si)(ai-Vref)\}$$

$$Cf101=\sum_{i=1}^{n}C101i \quad (7)$$

$$CC1=Cf102=\sum_{i=1}^{n}C102i \quad (8)$$

Instead of the circuits for summing up the total bits of the same weight with respect to each weight as shown in Figs.6, 7 and 13, a circuit can be used, in which outputs X'11 to X'1M from the exclusive-OR circuits XOR1 (Fig.8) are weighted, and similar calculations are performed for XOR2 to XORn, and the weighted addition results are summed up. This circuit is larger in circuit size due to increased weighted addition circuits and increased unit capacitances.

[0050] Fig.17 is a circuit diagram showing another analog adder for the third embodiment. The analog adder includes an adder 71R corresponding to the adder 7_1. The adder 71R includes a resistance coupling consisting of parallel resistances R11 to RN1 corresponding to C11 to CN1 outputs of which are commonly connected to an input of an inverting amplifier 81R. An output of the inverting amplifier 81R is connected through a feedback resistance Rf1 to its input. Here, inputs to the resistances R11 to RN1 are X'11 to X'N1, N · Rf1=R11=R21=...=RN1 , the output is defined as in the formula (9).

$$Vo101\text{-}Vb=-\frac{\sum_{i=1}^{N}\frac{(X'i1-Vb)}{Ri1}}{\frac{1}{Rf1}}=-\frac{\sum_{i=1}^{N}X'i1}{N}+Vb \quad (9)$$

A simple addition is performed.

[0051] Fig.18 is a circuit diagram showing an analog adder using weighted addition circuit 9R similar to the weighted addition circuit in Fig.8. The weighted addition circuit 9R includes a resistance coupling consisting of resistances R1 to RM corresponding to C1 to CM. An output of the resistance coupling is connected to thriugh a feedback resistance Rf to its input.

[0052] When inputs of the resistances R1t to RM are Vo101 to Vo10M, a relationship between MRf and R1 to PM is as in the formula (10). An output Aout is expressed as in the formula (11).

$$Rf=RM=2^{-1}RM\text{-}1=2^{-2}RM\text{-}21=...=2^{-(M-1)}R1 \quad (10)$$

$$Aout\text{-}Vb = -\frac{\sum_{i=1}^{N} \frac{(X'i1 - Vb)}{Ri1}}{\frac{1}{Rf1}} = -\sum_{i=1}^{M} 2^{i-1} \cdot Vo\,10\,i + Vb \qquad (11)$$

[0053] Fig.19 is a circuit diagram showing another analog adder using a MOS differential amplifier DAMP instead of the CMOS inverter-inverting amplifier. An output of DAMP is input to an inverted input, and non-inverted input is grounded. An output of DAMP is connected through a feedback capacitance CF13 to its input.

[0054] Fig.20 is a circuit diagram showing the MOS differential amplifier DAMP in Fig.19. The MOS differential amplifier includes two symmetric pairs of MOS transistors T131 and T133, and T132 and T134. The transistors T131 and T132 are connected at their gates with each other, and their gates are connected to a drain of the transistor T133. An input signal is input to a gate of the transistor T133, and a gate of the transistor T134 is grounded. A drain of the T134 is connected to an output terminal. A constant current source IS is disposed, to which a control signal SWV is input. The DAMP becomes sleep mode when IS is cut off by the control signal so that the electrical power consumption is stopped.

[0055] Fig.21 is a block diagram showing another embodiment of a signal reception apparatus for DS-CDMA cellular system using the above matched filter.

[0056] In Fig.21, an analog input signal Ain is passed through an A/D converter and is input to a matched filter as well as to sliding correlators SC1, SC2 and SC3 The matched filter is used for an initial acquisition of the input signal Ain, and after completing of the initial acquisition, demodulation is performed by the sliding correlators. The electric power consumption of the matched filter is reduced. The matched filter is intermittently used for tracking after the initial acquisition, or a delay-locked-loop (DLL) is used for the tracking. The power consumption can be decreased by DLL, however, the additional DLL makes the circuit size bigger. An output of the matched filter is input to a circuit 121 for frame synchronization during the initial acquisition. The circuit 121 outputs a signal to a circuit 122 for a code generation and a control which determines the synchronization timing of the sliding correlators SC1 to SC3. Output of the sliding correlators SC1 to SC3 are input to a circuit 123 for various processing such as rake combining. Since the sliding correlators are usually digital circuit, the digital input to the matched filter is preferable for the sliding correlators.

Claims

1. A matched filter for calculating a correlation between successive analog input signals and a spreading code consisting of a series of 1 bit data, comprising:

   an analog to digital (A/D) converter for converting said analog signals into digital data;
   one or more of data holding means each having a plurality of stages for holding said digital data in said stages;
   a multiplier supplying means for supplying said spreading code;
   a plurality of exclusive-OR circuits corresponding to said stages, each of which calculates an exclusive-OR of one of said digital data and on eof said 1 bit data; and
   an analog adder for summing said exclusive-ORs up.

2. A matched filter as claimed in Claim 1, wherein,

   a plurality of said data holding means are provided;
   said A/D converter receives said analog signals in response to a sampling clock of a multiple sampling rate corresponding to a number of said data holding means;
   each said data holding means is successively selected for outputting said analog signals to said exclusive-OR circuits; and
   said analog adder successively sums said exclusive-ORs corresponding to said data holding means selected.

3. A matched filter as claimed in Claim 2, wherein,

   each said data holding means is a plurality of data registers which receive said digital data successively and circulatedly in synchronism with said sampling clock;
   said plurality of data holding means are parallelly connected to said A/D converter, and one of said data holding means is successively selected for receiving said digital data synchronously to said sampling clock; and
   each said multiplier supplying means is a shift register which shifts and circulates said spreading code synchronously to said sampling clock so that a relationship between an order of said digital data and an order of

said spreading code is maintained.

4. A matched filter as claimed in Claim 2, wherein,

each said data holding means is a shift register which receives and shifts said digital data synchronously to said sampling clock; and
said multiplier supplying means comprises a register for holding said spreading code.

5. A matched filter as claimed in Claim 2, wherein,

said digital data is a signed digital data having a sign bit indicative of positive and negative of said analog signals; and
a section signal having two status is calculated by an exclusive-OR of said sign bit and said spreading code; and
said analog adder subtracts a summation of exclusive-ORs corresponding to one of said status of said selection signal from a summation of exclusive-ORs corresponding to the other status of said selection signal.

6. A matched filter as claimed in Claim 2, wherein said multiplier supplying means comprises a plurality of multiplier holding means which hold different spreading code, and one of which is selected for supplying said spreading code to said exclusive-OR circuits.

7. A matched filter as claimed in Claim 6, wherein said plurality of multiplier holding means are selected in a time-sharing manner, and said analog adder calculates a summation in a time-sharing manner synchronously to said selection of said multiplier holding means.

8. A matched filter as claimed in Claim 3, wherein one or more of said multiplier holding means outputs said spreading code shifted by one stage from said order for maintaining said relationship.

9. A matched filter as claimed in Claim 3, wherein each said exclusive-OR circuit outputs high level or low level voltage supplied from outside according to said exclusive-OR of said digital data and said spreading code.

10. A matched filter as claimed in Claim 2, wherein each said exclusive-OR circuit outputs a plurality of levels voltages supplied from outside according to a plurality of said exclusive-ORs.

11. A matched filter as claimed in Claim 3, wherein said analog adder comprises a plurality of analog sub-adders each of which corresponding to one of weights of bits of said outputs from said exclusive-OR circuits, and each said sub-adder sums said bits of said corresponding weight up, and said analog adder further comprises a weighted adder for weighting said outputs of said sub-adders and for summing them up.

12. A matched filter as claimed in Claim 3, wherein said analog adder comprises a plurality of weighted adders for weighting said outputs of said exclusive-OR circuits and summing them up, and an adder for summing outputs of said weighted adders.

13. A matched filter as claimed in Claim 3, wherein said analog adder comprises a capacitive coupling including a plurality of capacitances inputs thereof are connected input voltages, an inverting amplifier-input of which is commonly connected to outputs of said capacitances, and a feedback capacitance connected between an output and said input of said inverting amplifier, whereby said weighting addition and said summation are performed.

14. A matched filter as claimed in Claim 3, wherein said analog adder comprises a resistance coupling including a plurality of resistances inputs thereof are connected input voltages, an inverting amplifier input of which is commonly connected to outputs of said resistances, and a feedback reistance connected between an output and said input of said inverting amplifier, whereby said weighting addition and said summation are performed.

15. A matched filter as claimed in Claims 13 and 14, wherein said inverting amplifier comprises a plurality of CMOS inverters serially connected.

16. A matched filter as claimed in Claims 13 and 14, wherein said inverting amplifier comprises a COM differential amplifier.

17. A matched filter as claimed in Claims 13 and 14, wherein said inverting amplifier becomes sleep mode by a control from outside.

18. A signal reception apparatus of DS-CDMA communication system using a matched filter for a correlation calculation between successive analog input signals and a spreading code consisting of a series of 1 bit data, said matched filter comprising:

an analog to digital (A/D) converter for converting said analog signals into digital data;
one or more of data holding means each having a plurality of stages for holding said digital data in said stages;
a multiplier supplying means for supplying said spreading code;
a plurality of exclusive-OR circuits corresponding to said stages, each of which calculates an exclusive-OR of one of said digital data and on eof said 1 bit data; and
an analog adder for summing said exclusive-ORs up.

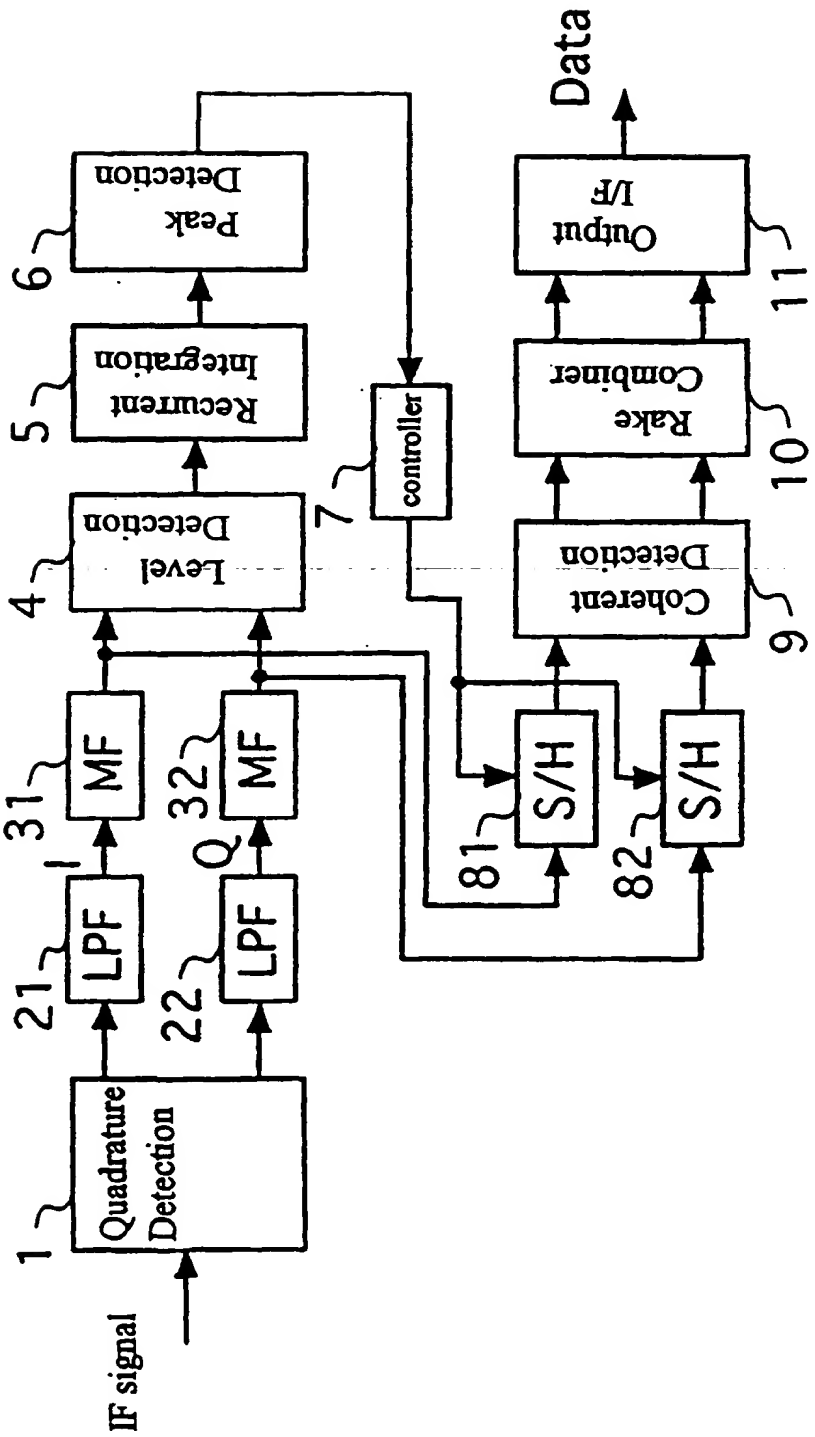
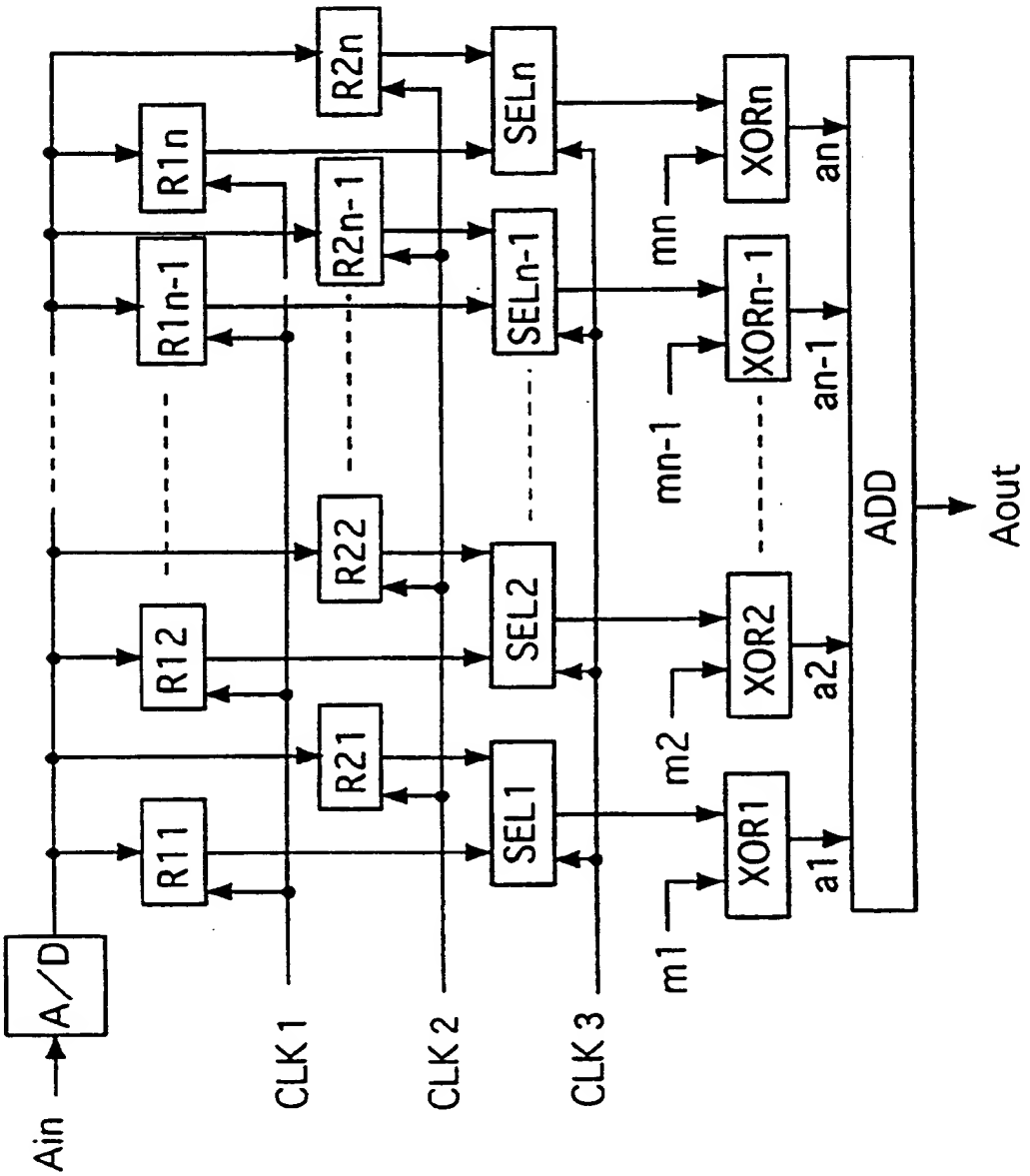


Fig.1

Fig.2



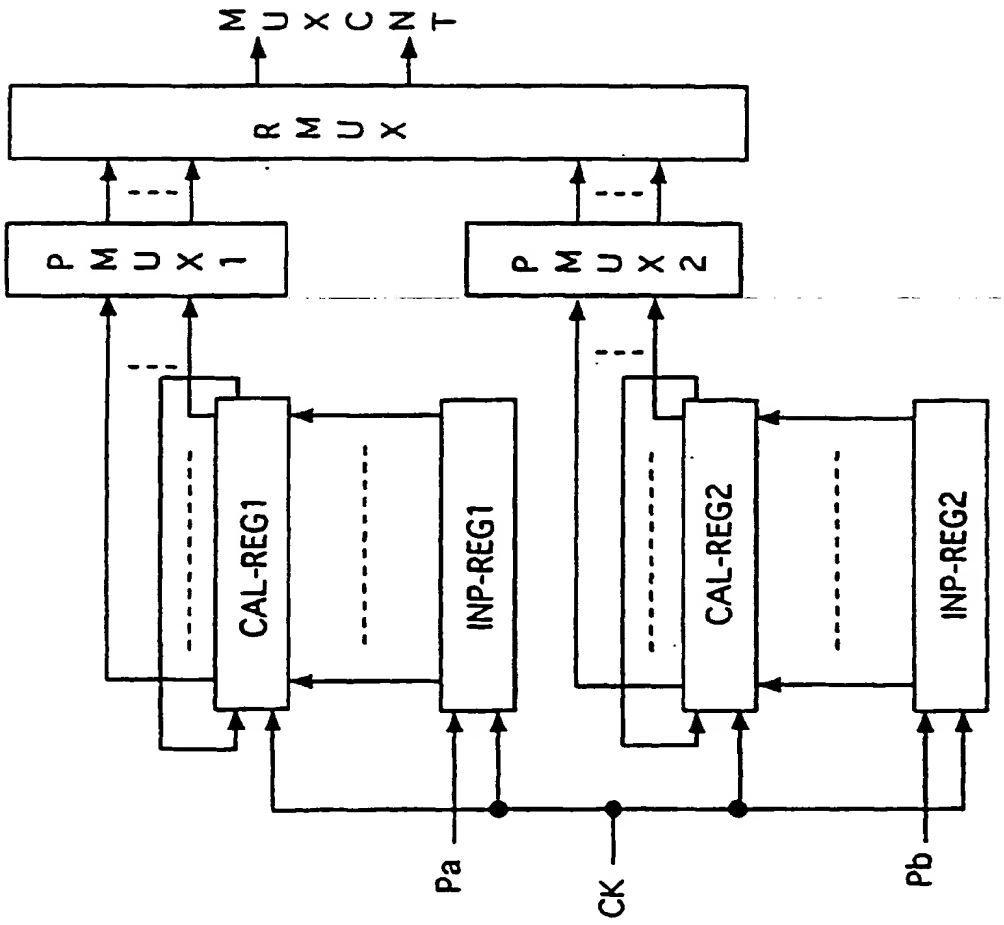


Fig.3

Fig.4

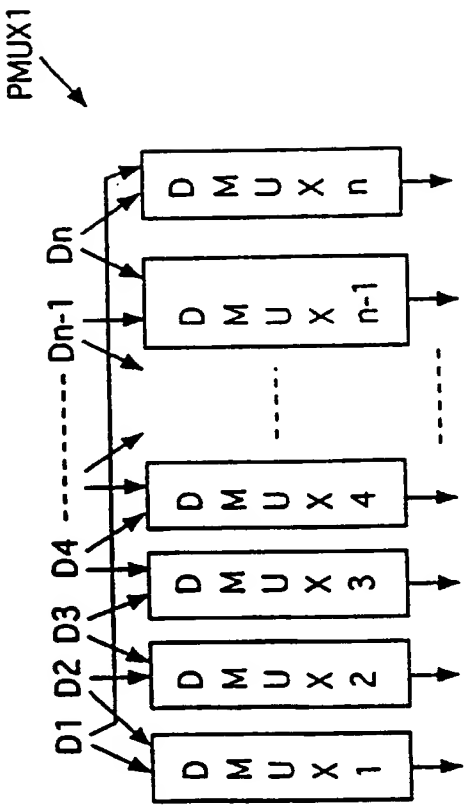


Fig.5

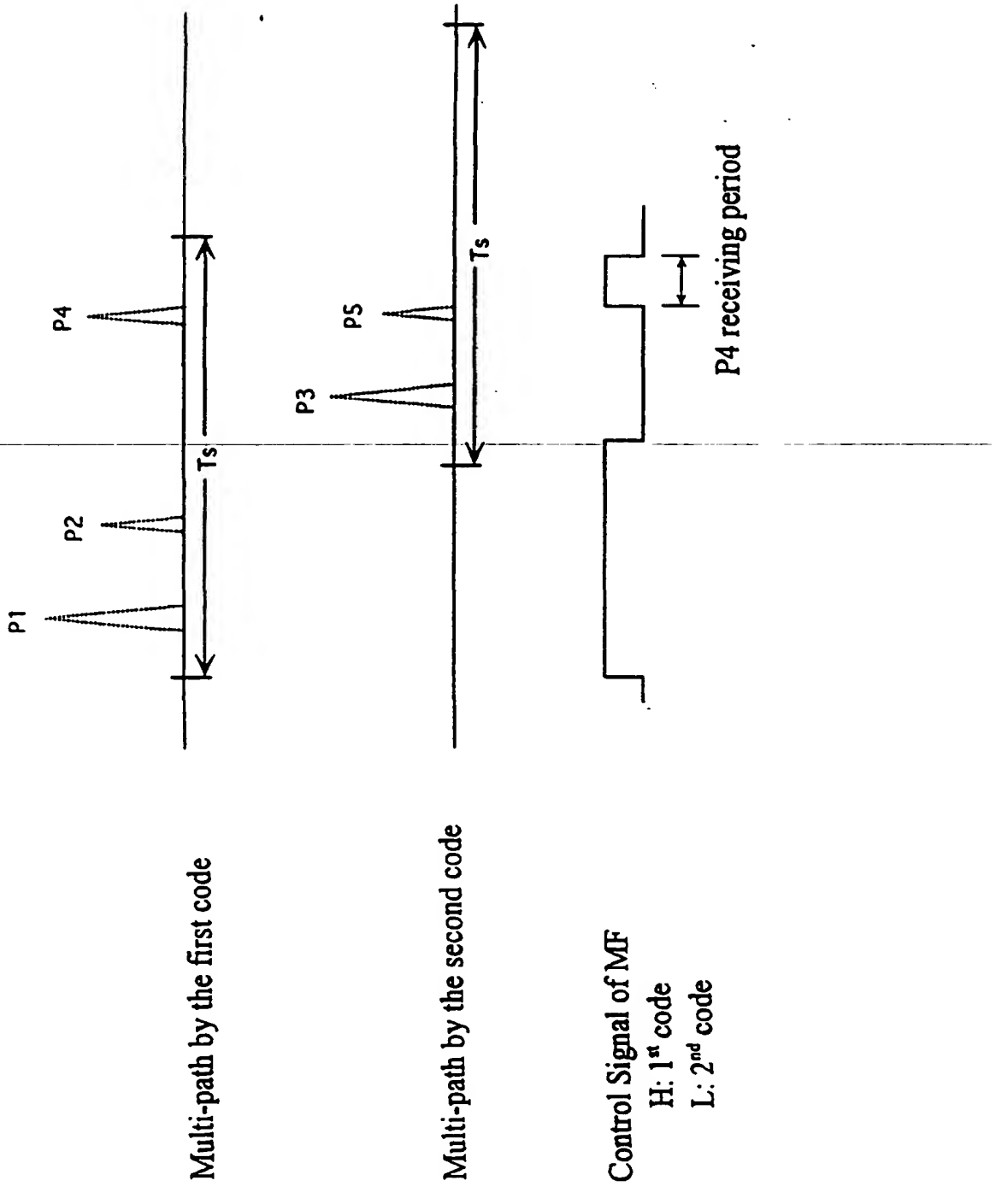
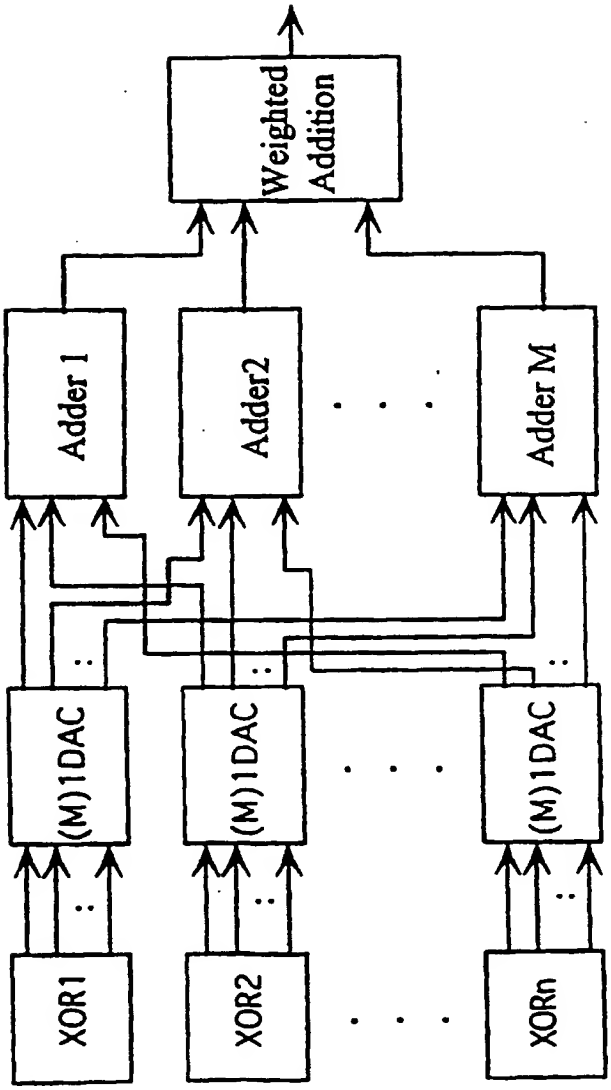


Fig.6



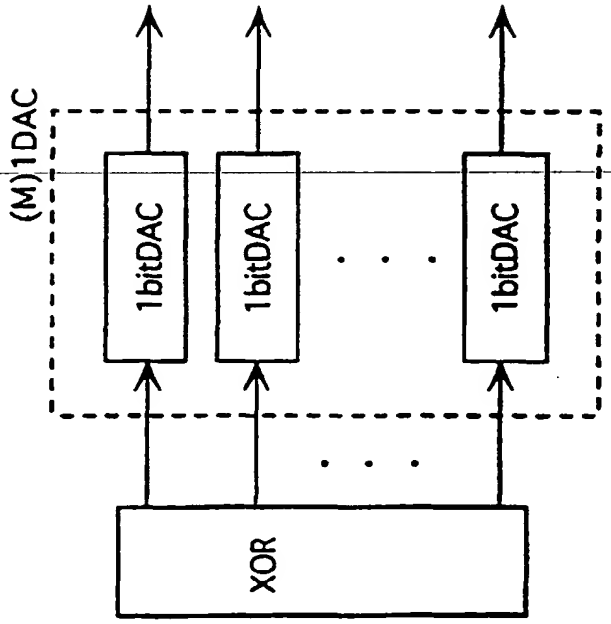


Fig.7

Fig.8

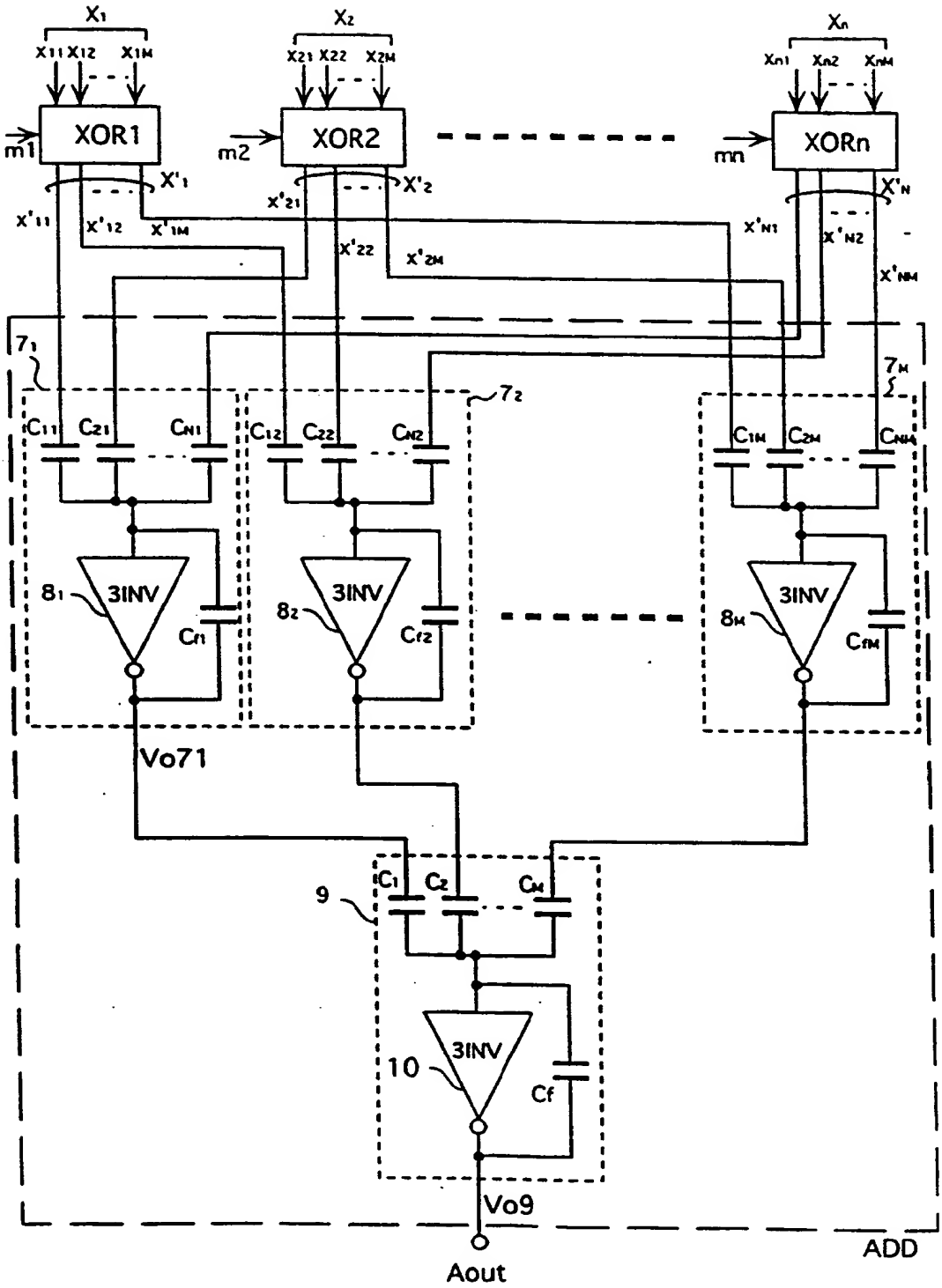


Fig.9

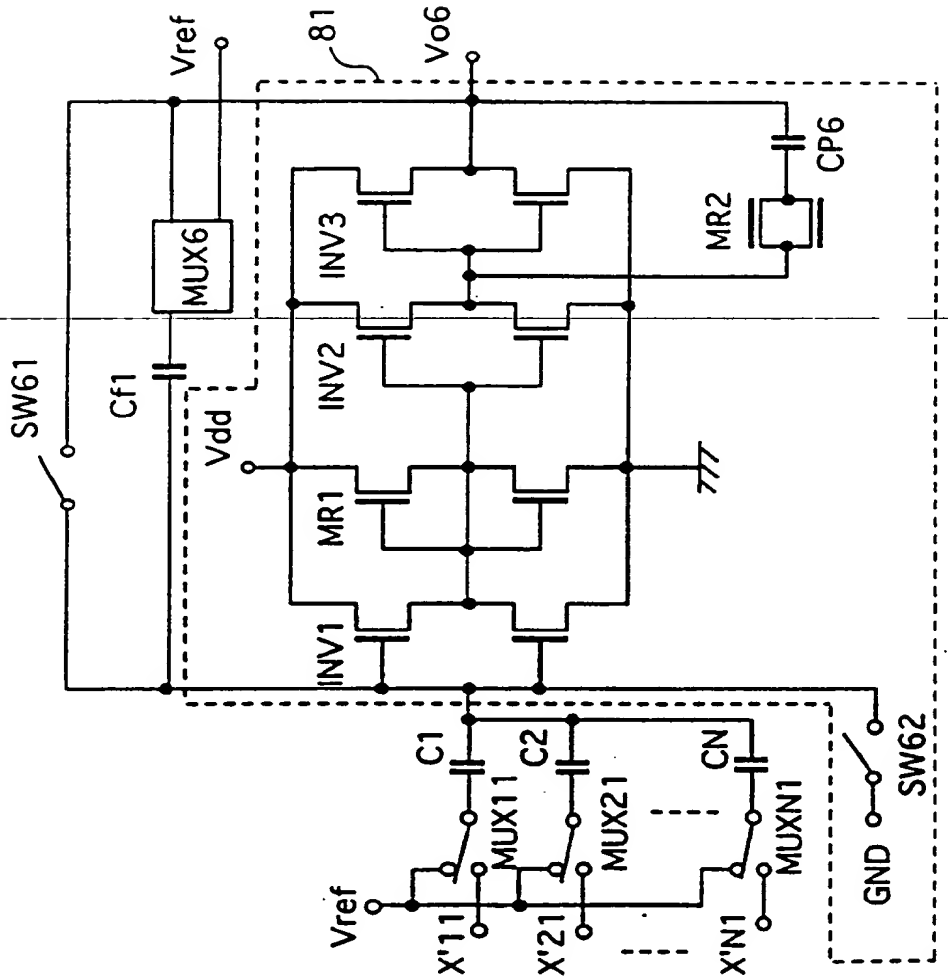


Fig.10

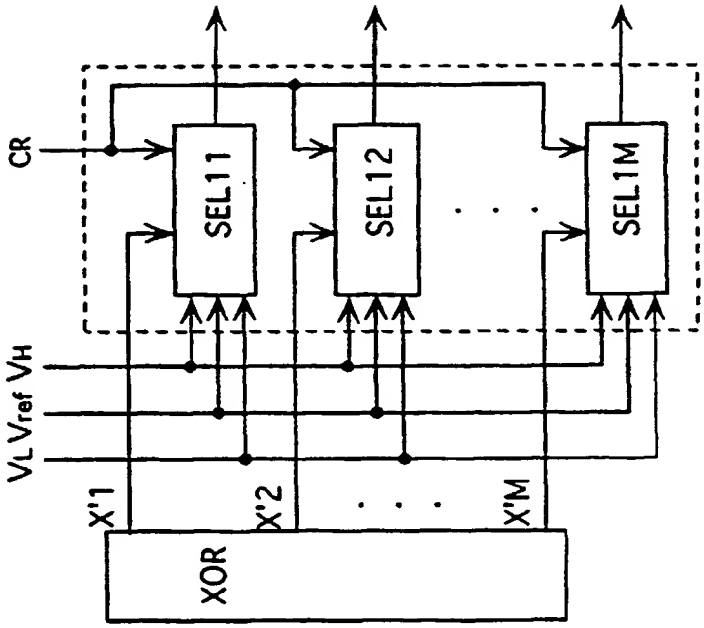


Fig.11

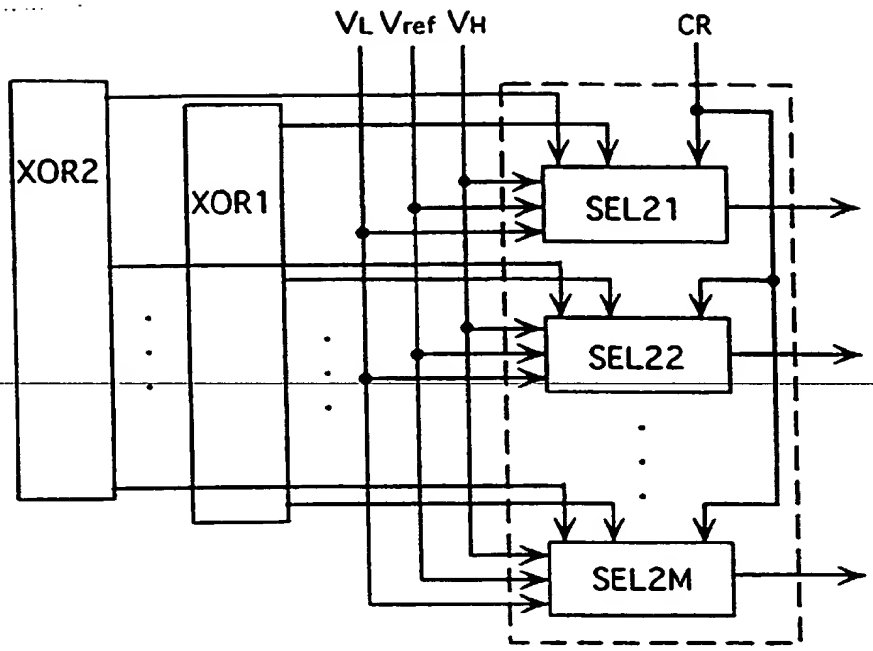


Fig.12

X1	X2	Out
1	1	VH
1	0	Vref
0	1	Vref
0	0	VL

Fig.13

ME

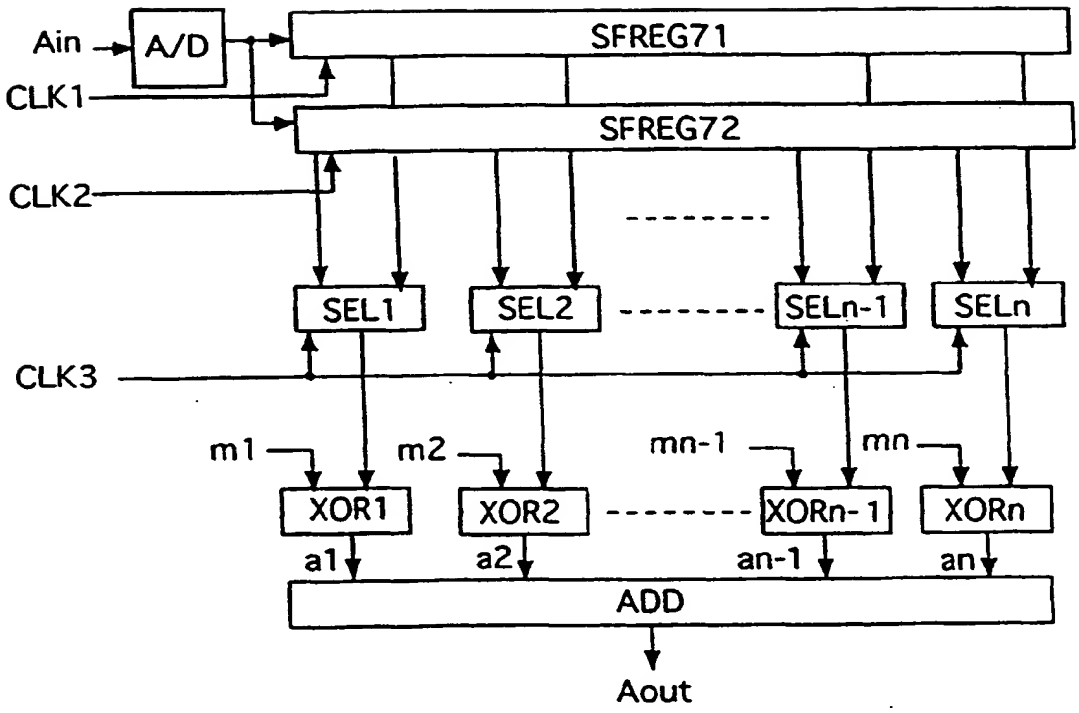


Fig.14

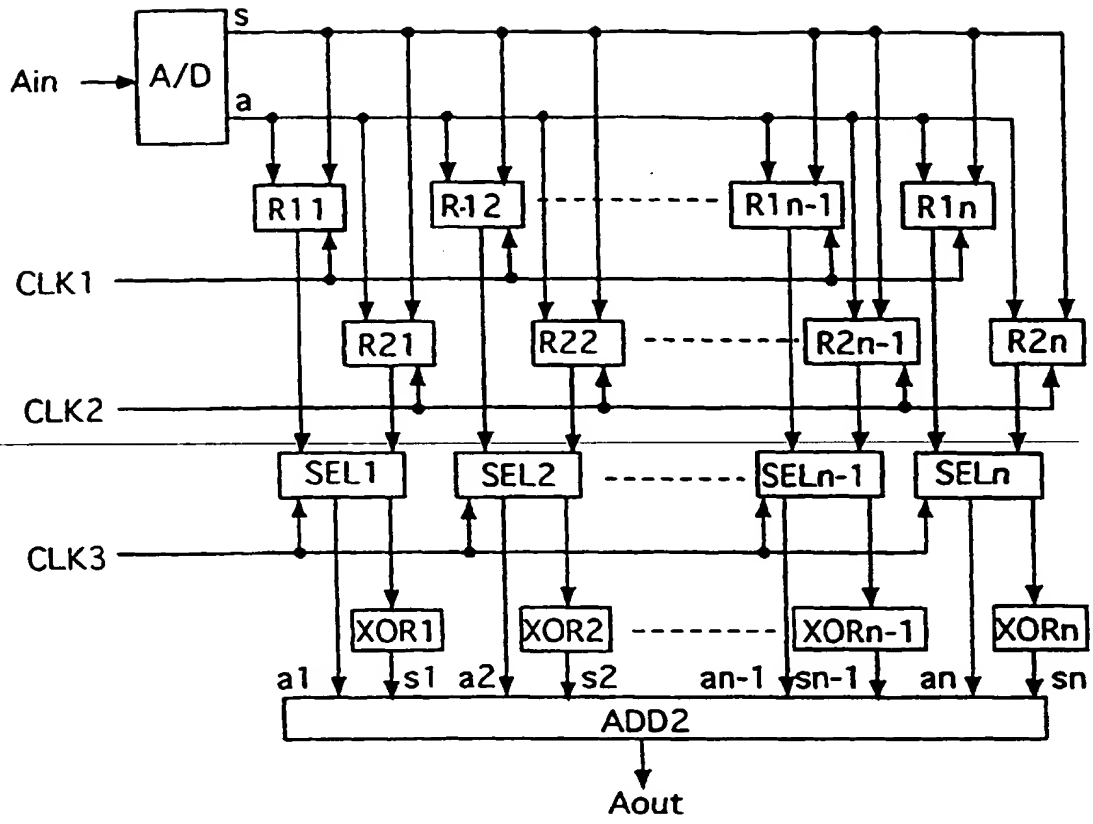


Fig.15

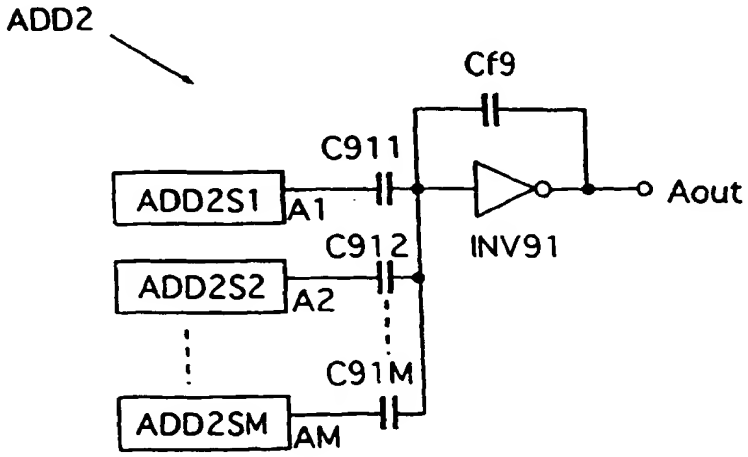


Fig.16

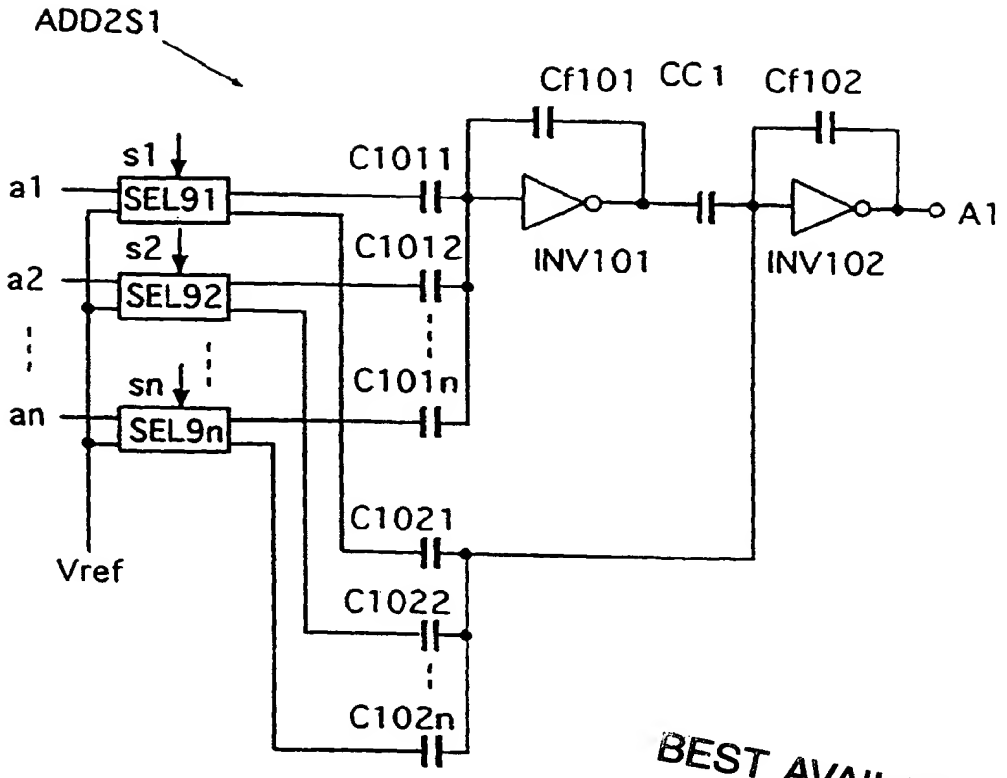


Fig.17

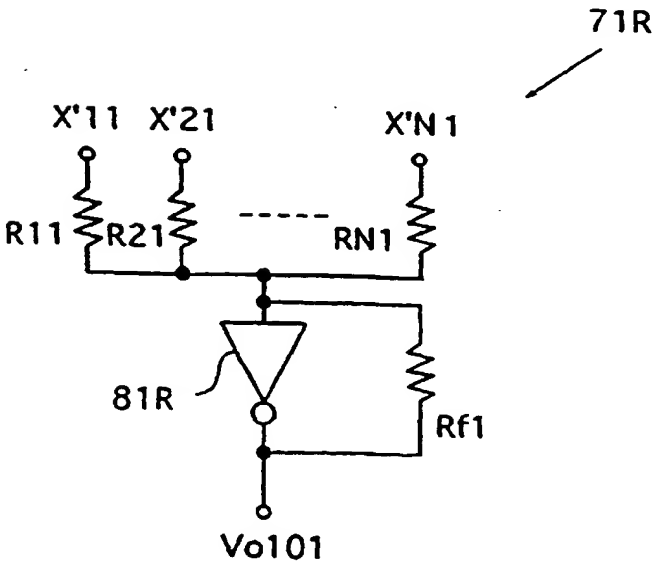


Fig.18

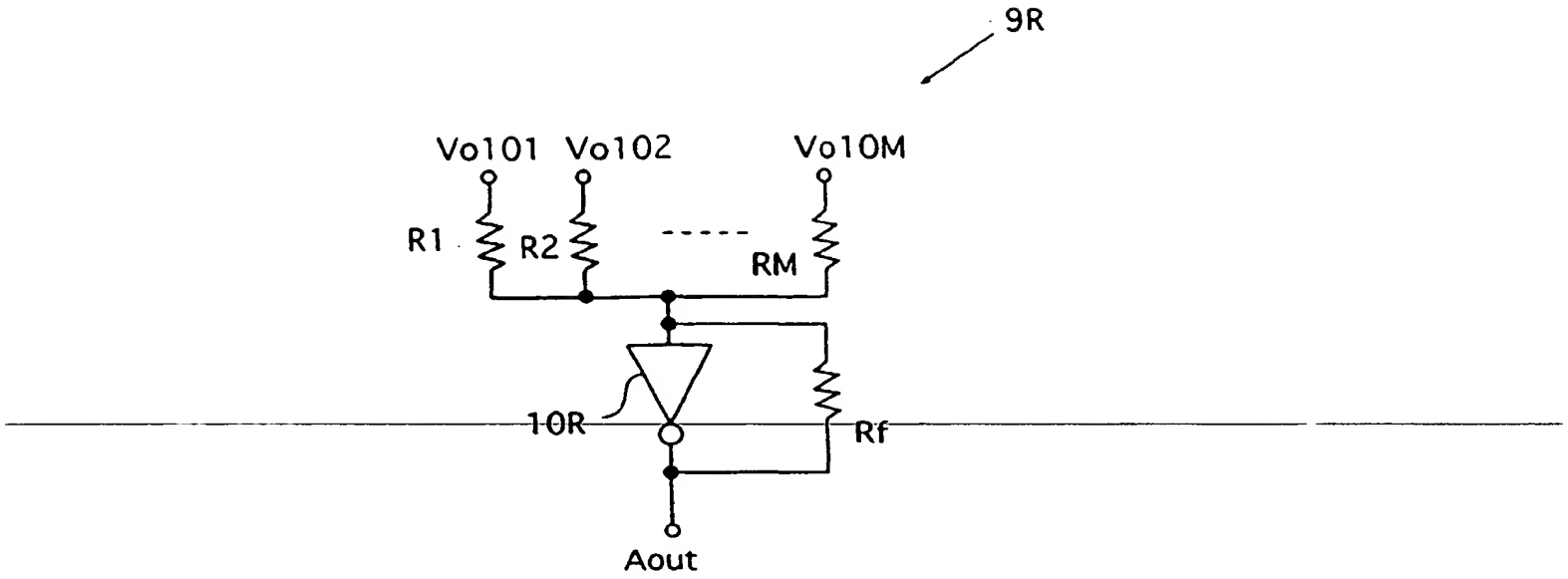


Fig.19

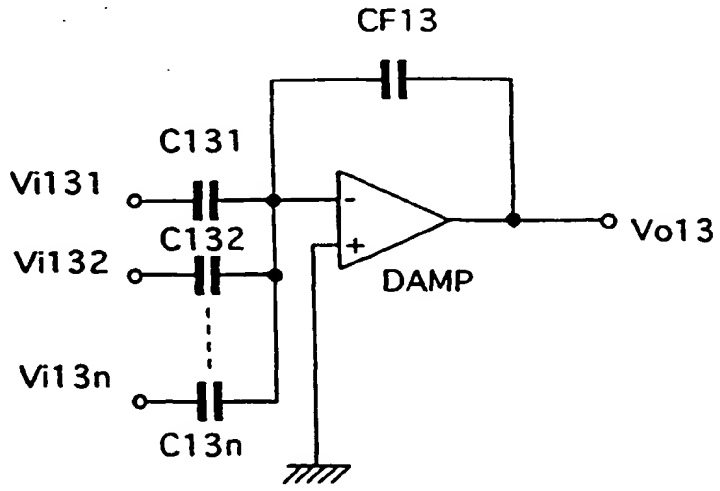


Fig.20

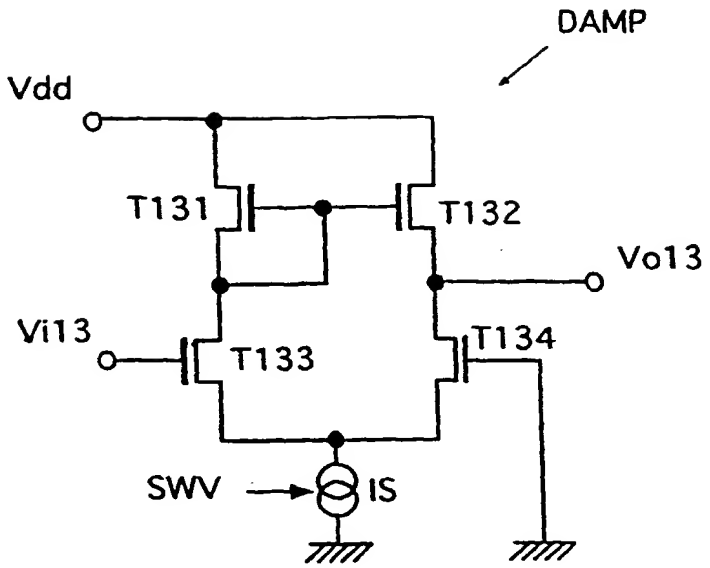
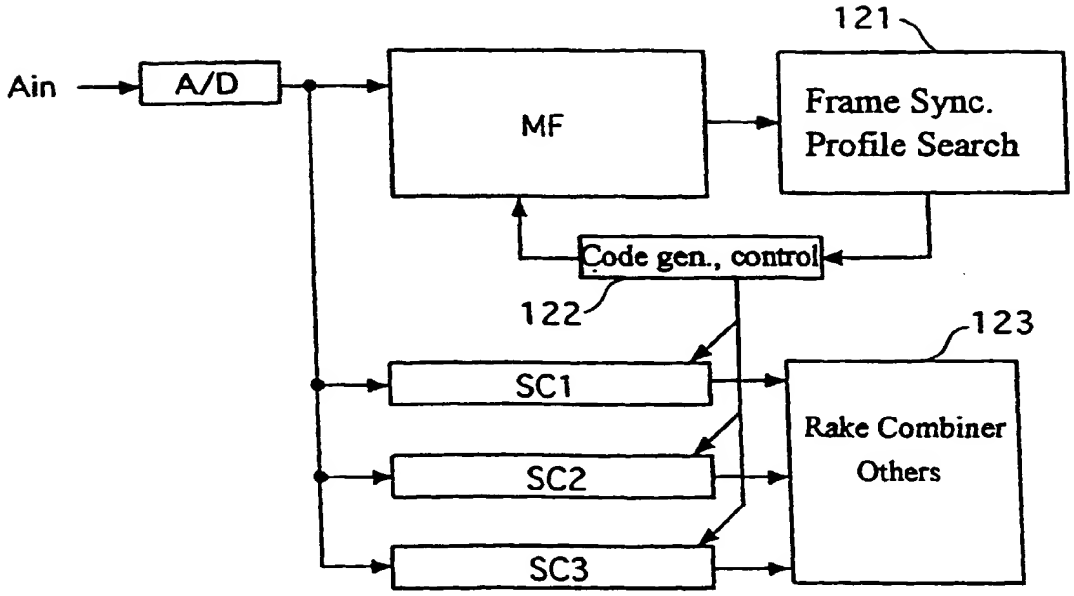


Fig.21



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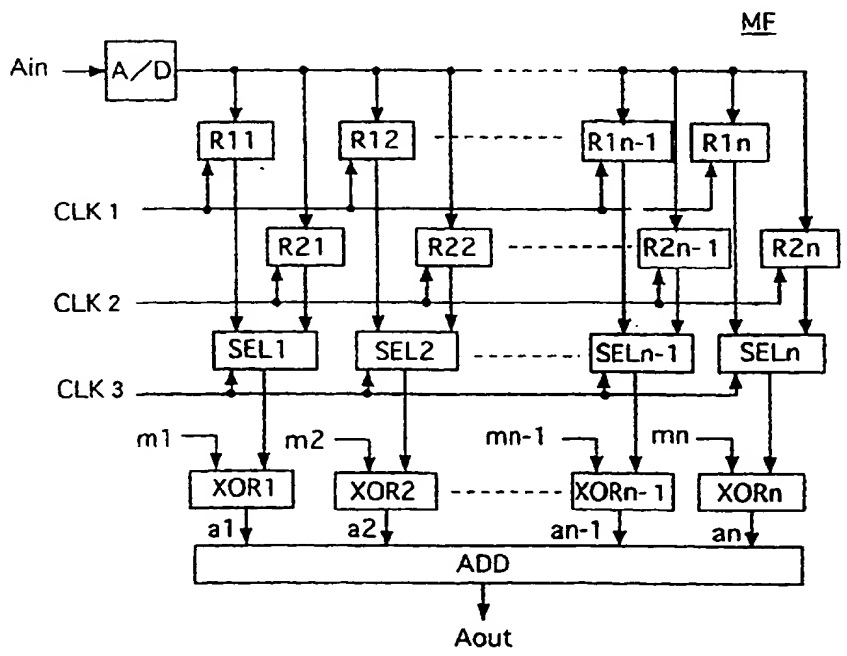
(54) Matched filter and signal reception apparatus

(57) An analog input signal is converted into digital data by an A/D converted, a digital multiplication as a correlation calculation is executed by a plurality of exclusive-OR circuits, and an analog addition of outputs of the exclusive-OR circuits is performed. In the multiplication, the digital data is multiplied a spreading code of one bit. The exclusive-OR outputs are added for each weight of bits, and the addition results are weighted and summed up.

Fig.2



EP 0 939 500 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 99 10 3383

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	7 February 2003	Russo, M

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